FAIRCHILD SEMICONDUCTOR®

March 2008

SG6860
Low-Cost, Green-Mode PWM Controller for Flyback Converters

Features

- Green-Mode PWM
- Supports the “Blue Angel” Eco Standard
- Low Start-up Current: 9µA
- Low Operating Current: 3mA
- Leading-Edge Blanking
- Constant Output Power Limit
- Universal Input
- Built-in Synchronized Slope Compensation
- Current Mode Operation
- Cycle-by-cycle Current Limiting
- Under-Voltage Lockout (UVLO)
- Programmable PWM Frequency with Frequency Hopping
- V_{DD} Over-Voltage Protection (Latch off)
- Gate Output Voltage Clamped at 17V
- Low Cost
- Few External Components Required
- Small SOT-26 Package

Applications

- Power Adaptors
- Open-Frame SMPS

Description

This highly integrated PWM controller provides several enhancements designed to meet the low standby-power needs of low-power SMPS. To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. This green-mode function enables the power supply to meet even strict power conservation requirements.

The BiCMOS fabrication process enables reducing the start-up current to 9µA and the operating current to 3mA. To further improve power conservation, a large start-up resistance can be used. Built-in synchronized slope compensation ensures the stability of peak current mode control. Proprietary internal compensation provides a constant output power limit over a universal AC input range ($90V_{AC}$ to $264V_{AC}$). Pulse-by-pulse current limiting ensures safe operation even during short-circuits.

To protect the external power MOSFET from being damaged by supply over voltage, the SG6860’s output driver is clamped at 17V. SG6860 controllers can improve the performance and reduce the production cost of power supplies. The SG6860 can replace linear and RCC-mode power adapters. It is available in 8-pin DIP and 6-pin SOT-26 packages.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
SG6860TZ	-40°C to +85°C	Small SOT-26 Package	Tape & Reel
SG6860DZ	-40°C to +85°C	8-pin Dual in-line Package (DIP)	Rail

All packages are lead free per JEDEC: J-STD-020B standard.

Application Diagram

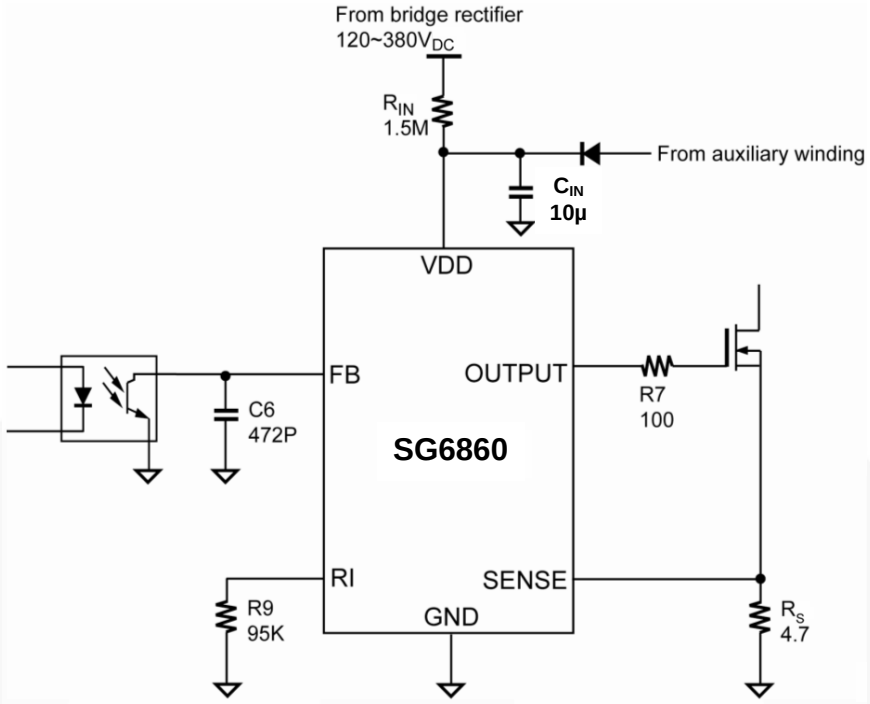

Figure 1. Typical Application

Block Diagram

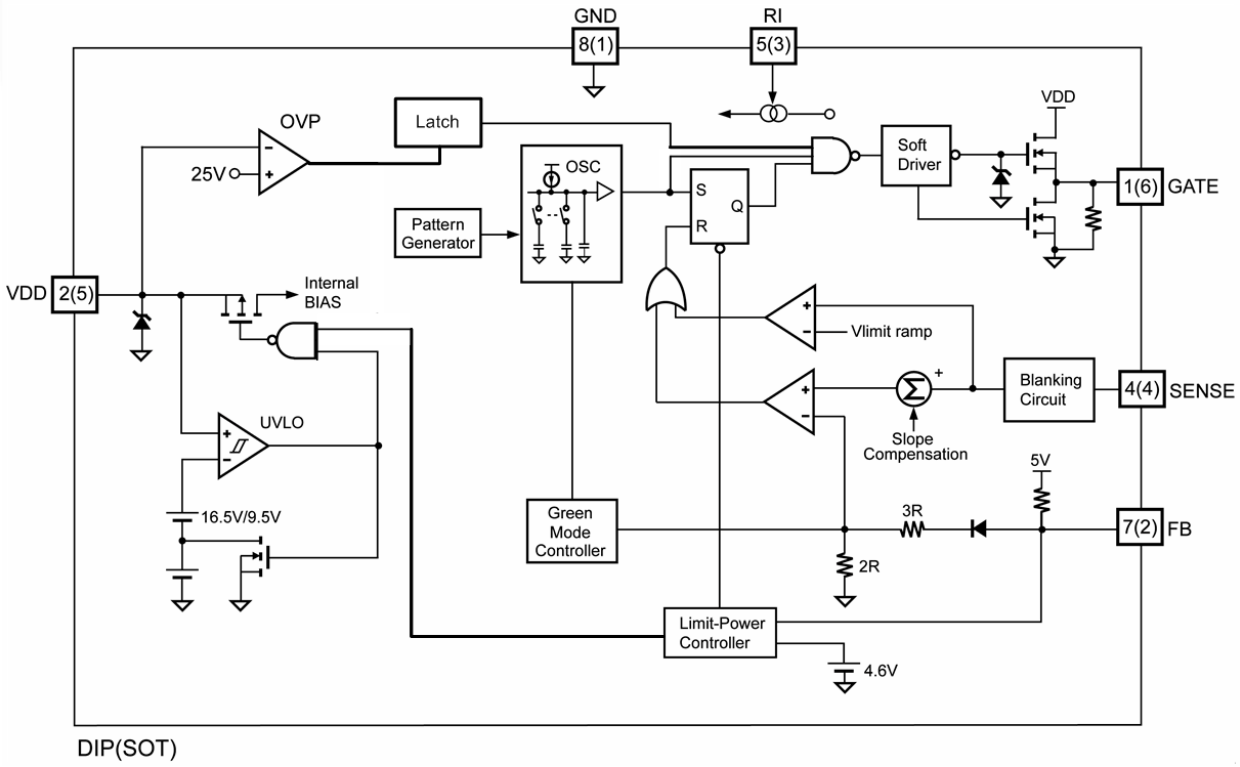

Figure 2. Function Block Diagram

Pin Configuration

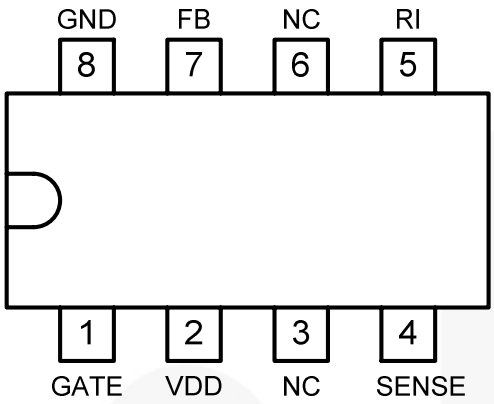

Figure 3. DIP Pin Configuration (Top View)

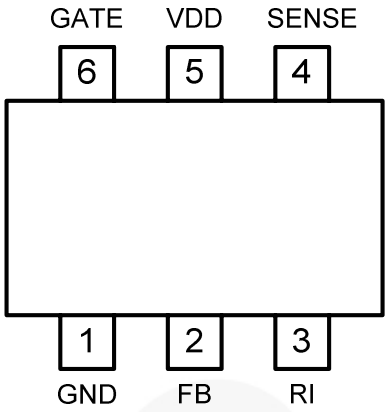

Figure 4. SOT Pin Configuration (Top View)

Pin Definitions

Pin # DIP	Pin # (SOT)	Name	Description
1	(6)	GATE	**Driver Output**. The totem-pole output driver for driving the power MOSFET.
2	(5)	VDD	**Power Supply**.
3	--	NC	**No Connection**.
4	(4)	SENSE	**Current Sense**. This pin senses the voltage across a resistor. When the voltage reaches the internal threshold, PWM output is disabled, which activates over-current protection. This pin also provides current amplitude data for current-mode control.
5	(3)	RI	**Reference Setting**. A resistor connected from the RI pin to ground generates a constant current source used to charge an internal capacitor and determine the switching frequency. Increasing the resistance reduces the amplitude of the current source and reduces the switching frequency. A 95kΩ resistor, R_I, results in a 13μA constant current, I_I, and a 70kHz switching frequency.
6	--	NC	**No Connection**.
7	(2)	FB	**Feedback**.
8	(1)	GND	**Ground**. For ATX SMPS, it detects AC line voltage through the main transformer.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{VDD}	DC Supply Voltage			30	V
V_{FB}	Input Voltage to FB Pin		-0.3	7.0	V
V_{SENSE}	Input Voltage to Sense Pin		-0.3	7.0	V
P_D	Power Dissipation			300	mW
T_J	Operating Junction Temperature			+150	°C
θ_{JA}	Thermal Resistance (Junction-to-Air)	SOT		208.4	°C/W
		DIP		82.5	°C/W
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 seconds)			+260	°C
ESD	Electrostatic Discharge Capability, Human Body Model			3.5	KV
	Electrostatic Discharge Capability, Machine Model			200	V

Notes:
1. All voltage values, except differential voltage, are given with respect to GND pin.
2. Stresses beyond those listed under “absolute maximum ratings“ may cause permanent damage to the device.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Ambient Temperature	-40		+85	°C

Electrical Characteristics

V_{DD} =15V, T_A= 25°C, unless noted operating specs.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD} Section						
V_{DD-OP}	Continuous Operation Voltage				22	V
V_{DD-ON}	Turn-on Threshold Voltage		15.5	16.5	17.5	V
V_{DD-OFF}	Turn-off Threshold Voltage		8.5	9.5	10.5	V
I_{DD-ST}	Start-up Current	$V_{DD}=V_{DD-ON}$ – 0.1V		9	15	µA
I_{DD-OP}	Operating Supply Current	V_{DD}=15V, GATE with 1nF to GND		3.0	3.5	mA
V_{DD-OVP}	V_{DD} Over-voltage Protection Level	Latch off	24	25	26	V
$t_{D-VDDOVP}$	V_{DD} Over-voltage Protection Debounce	Latch off		120		µs
I_{DD-H}	Holding Current after OVP Latch-off	V_{DD}=5V	40	50	60	µA
Feedback Input Section						
Z_{FB}	Input Impedance			5		KΩ
$V_{FB-OPEN}$	FB Output High Voltage		5			V
V_{FB-OL}	FB Open-loop Trigger Level			4.7		V
t_{D-OLP}	Delay Time of FB Pin Open-loop Protection			54		ms
V_{FB-N}	Green-Mode Entry FB Voltage		2.60	2.85	3.10	V
V_{FB-G}	Green-Mode Ending FB Voltage			2.2		V
S_G	Green-Mode Modulation Slope	R_I=95KΩ	40	75	100	Hz/mV
Current-Sense Section						
Z_{SENSE}	Input Impedance		10			KΩ
t_{PD}	Delay to Output		40	55	100	ns
V_{STHFL}	Flat Threshold Voltage for Current Limit			1		V
V_{STHVA}	Valley Threshold Voltage for Current Limit		0.65	0.70	0.75	V
t_{LEB}	Leading-Edge Blanking Time		250	300	350	ns
DCY_{SAW}	Duty Cycle of SAW Limit	Maximum Duty Cycle		40		%
Oscillator Section						
f_{OSC}	Center Frequency	R_I=95KΩ	65	70	75	KHz
	Hopping Range			±4.9		
t_{HOP}	Hopping Period	R_I=95KΩ		3.7		ms
f_{OSC-G}	Green-Mode Frequency	R_I=95KΩ		20		KHz
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=13.5 to 22V	0	0.02	2.00	%
f_{DT}	Frequency Variation vs. Temperature Deviation	T_A=-20 to 85°C			2	%
Output Section						
DCY_{MAX}	Maximum Duty Cycle		70	75	80	%
V_{GATE-L}	Output Voltage Low	V_{DD}=15V, I_O=20mA			1.5	V
V_{GATE-H}	Output Voltage High	V_{DD}=13.5V, I_O=20mA	8			V
t_r	Rising Time	V_{DD}=15V, C_L=1nF		135		ns
t_f	Falling Time	V_{DD}=15V, C_L=1nF		35		ns
$V_{GATE-CLAMP}$	Output Clamp Voltage	V_{DD}=22V	16	17	18	V

Typical Performance Characteristics

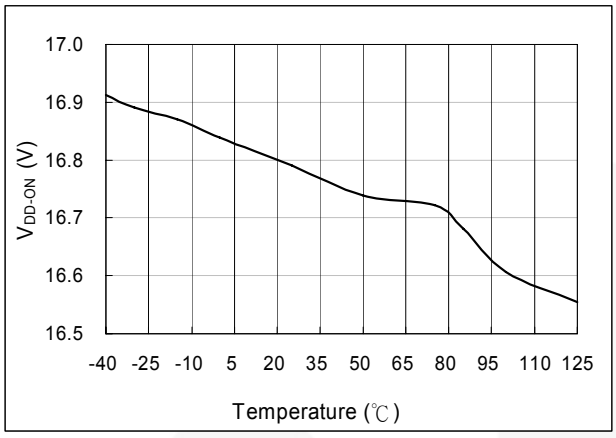

Figure 5. V_{DD-ON} vs. T_A

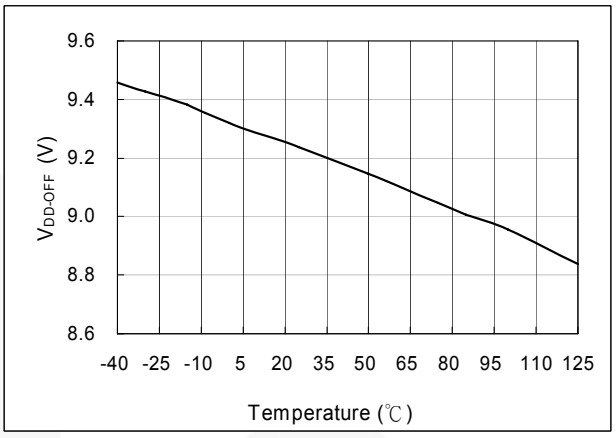

Figure 6. V_{DD-OFF} vs. T_A

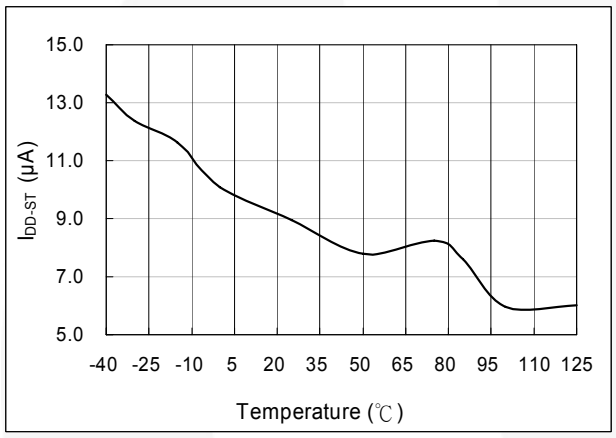

Figure 7. I_{DD-ST} vs. T_A

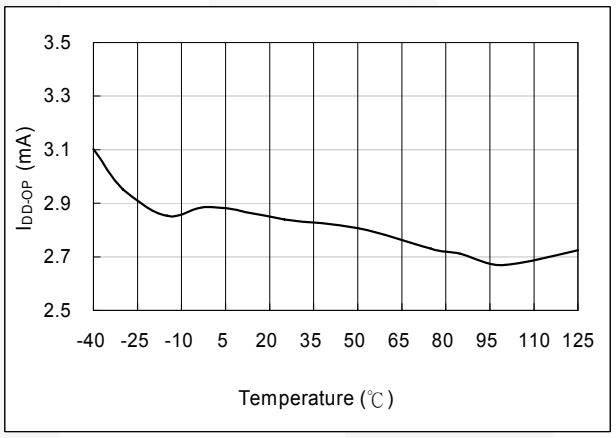

Figure 8. I_{DD-OP} vs. T_A

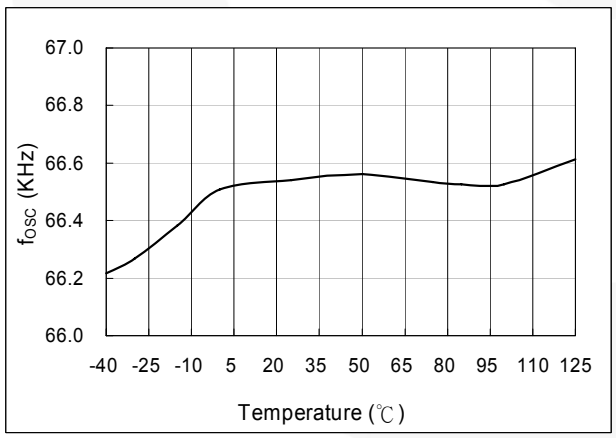

Figure 9. f_{OSC} vs. T_A

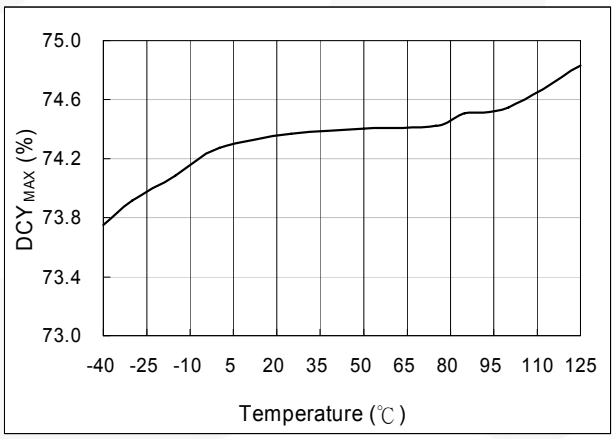

Figure 10. DCY_{MAX} vs. T_A

Typical Performance Characteristics (Continued)

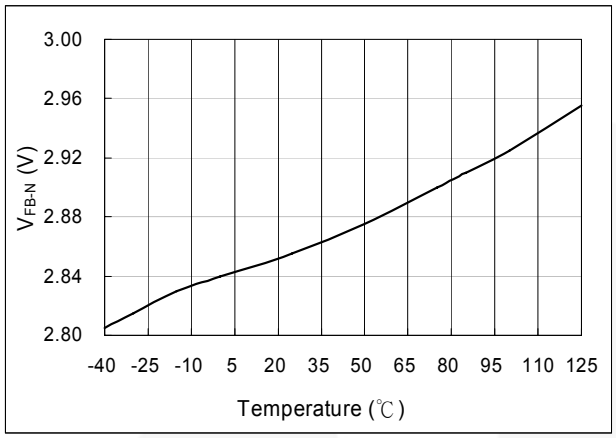

Figure 11. V_{FB-N} vs. T_A

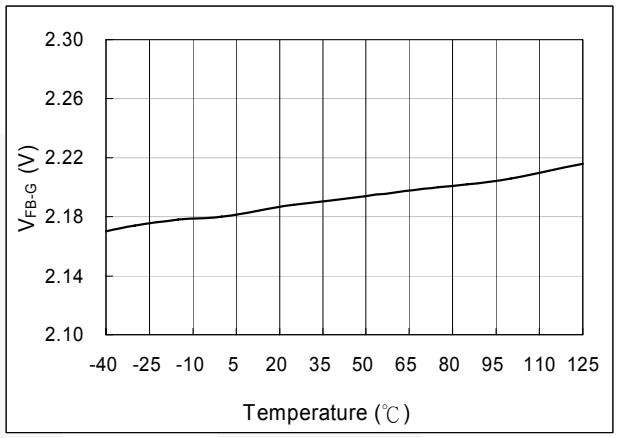

Figure 12. V_{FB-G} vs. T_A

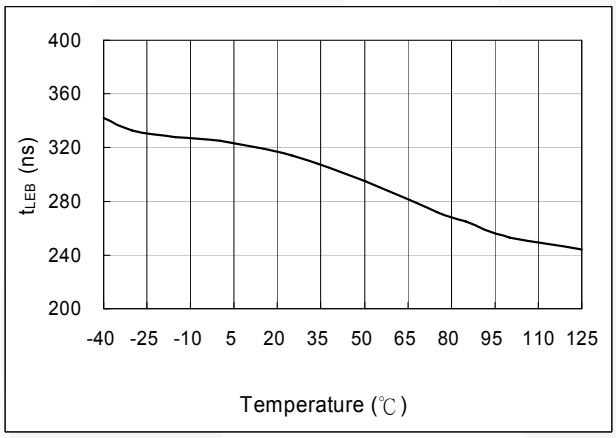

Figure 13. t_{LEB} vs. T_A

Functional Description

SG6860 integrates many useful designs into one controller for low-power switch-mode power supplies. The following descriptions highlight some of the features of the SG6860 series.

Start-up Current

The start-up current is only 9μA, which allows a start-up resistor with high resistance and low-wattage to supply the start-up power for the controller. A 1.5MΩ, 0.25W, start-up resistor and a 10μF/25V V_{DD} hold-up capacitor are sufficient for an AC-to-DC power adapter with a wide input range of $90V_{AC}$ to $264V_{AC}$.

Operating Current

The operating current has been reduced to 3mA, which results in higher efficiency and reduces the V_{DD} hold-up capacitance requirement.

Green-Mode Operation

The proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. On-time is limited to provide stronger protection against brownouts and abnormal conditions. The feedback current, which is sampled from the voltage feedback loop, is taken as the reference. Once the feedback current exceeds the threshold current, the switching frequency starts to decrease. This green-mode function dramatically reduces power consumption under light-load and zero-load conditions. Power supplies using the SG6860 can meet even strict regulations regarding standby power consumption.

Oscillator Operation

A resistor connected from the RI pin to ground generates a constant current source used to charge an internal capacitor. The charge time determines the internal clock speed and the switching frequency. Increasing the resistance reduces the amplitude of the input current and reduces the switching frequency. A 95kΩ resistor, R_I, results in a 13μA constant current, I_I, and a 70kHz switching frequency. The relationship between R_I and the switching frequency is:

$$f_{PWM} = \frac{6650}{R_I(k\Omega)}(kHz) \quad (1)$$

The range of the oscillation frequency is designed to be within 50kHz ~ 100kHz.

Leading-Edge Blanking

Each time the power MOSFET is switched on, a turn-on spike occurs at the sense-resistor. To avoid premature termination of the switching pulse, a 300ns leading-edge blanking time is built in. Conventional RC filtering can therefore be omitted. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Constant Output Power Limit

When the SENSE voltage across the sense resistor, R_S, reaches the threshold voltage (~1.00V), the output GATE drive is turned off after propagation delay, t_{PD}. This propagation delay introduces an additional current proportional to $t_{PD} \bullet V_{IN}/L_p$. The propagation delay is nearly constant, regardless of the input line voltage V_{IN}. Higher input line voltages result in larger additional currents. At high input line voltages, the output power limit is higher than at low input line voltages.

To compensate for this output power limit variation across a wide AC input range, the threshold voltage is adjusted by adding a positive ramp. This ramp signal rises from 0.70V to 1.00V, then flattens out at 1.00V. A smaller threshold voltage forces the output GATE drive to terminate earlier. This reduces the total PWM turn-on time and makes the output power equal to that of low line input. This proprietary internal compensation ensures a constant output power limit for a wide AC input voltage range ($90V_{AC}$ to $264V_{AC}$).

Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16.5V and 9.5V. During start-up, the hold-up capacitor must be charged to 16.5V through the start-up resistor to enable SG6860. The hold-up capacitor continues to supply V_{DD} until power can be delivered from the auxiliary winding of the main transformer. V_{DD} must not drop below 9.5V during the start-up process. This UVLO hysteresis window ensures that the hold-up capacitor is adequate to supply V_{DD} during start-up.

Gate Output

The SG6860 BiCMOS output stage is a fast totem pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 17V Zener diode to protect power MOSFET transistors against undesired over-voltage gate signals.

Built-in Slope Compensation

The sensed voltage across the current sense resistor is used for current mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillations due to peak current mode control. The SG6860 has a synchronized, positively-sloped ramp built-in at each switching cycle. The slope of the ramp is:

$$\frac{0.36 \times Duty}{Duty(max.)} \quad (2)$$

Noise Immunity

Noise from the current sense or the control signal can cause significant pulse-width jitter, particularly in continuous-conduction mode. While slope compensation helps alleviate these problems, further precautions should be taken. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the SG6860, and increasing power MOS gate resistance improve performance.

Mechanical Dimensions

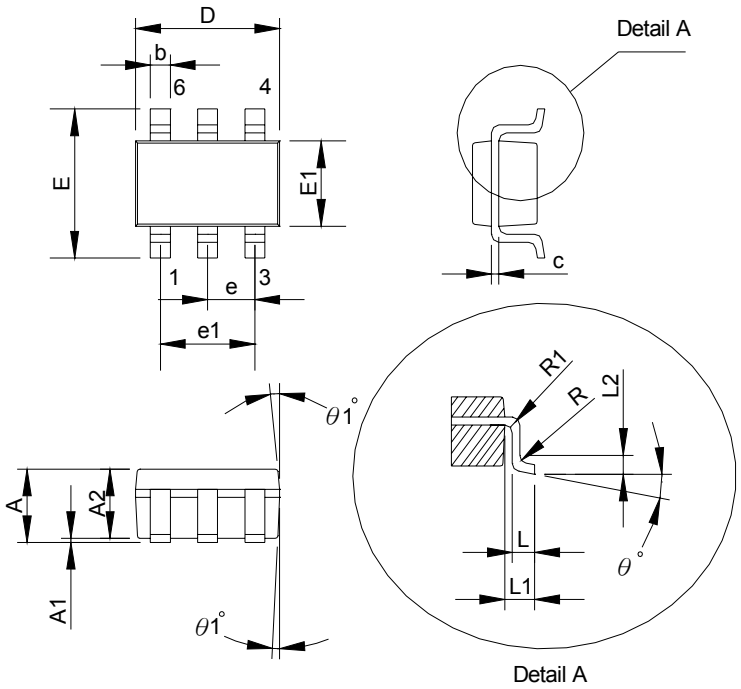

Figure 14. 6-SOTIC

Dimensions

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.45			0.057
A1			0.15			0.006
A2	0.76	1.03	1.30	0.030	0.041	0.051
b	0.30		0.50	0.011		0.020
c	0.08		0.22	0.003		0.009
D		2.90			0.114	
E		2.80			0.110	
E1		1.60			0.063	
e		0.95			0.037	
e1		1.90			0.075	
L	0.30	0.45	0.60	0.020	0.018	0.024
L1		0.60			0.024	
L2		0.25			0.010	
R1	0.10			0.004		
R2	0.10		0.25	0.004		0.010
θ°	0°	4°	8°	0°	4°	8°
θ1°	5°	10°	15°	5°	10°	15°

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/

Mechanical Dimensions (Continued)

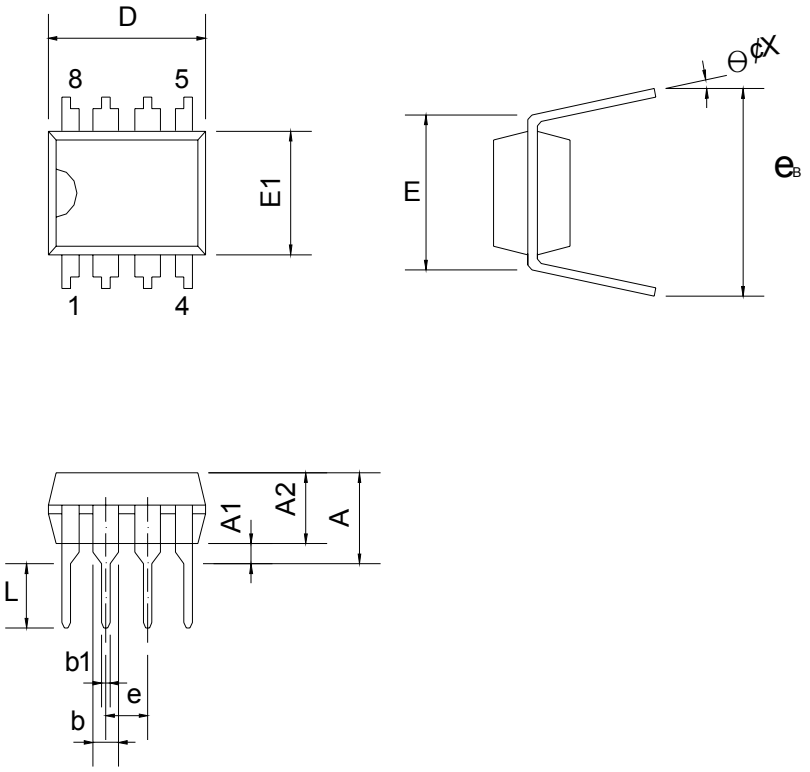

Figure 15. 8-DIPIC

Dimensions

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	9.017	9.271	10.160	0.355	0.365	0.400
E		7.620			0.300	
E1	6.223	6.350	6.477	0.245	0.250	0.255
e		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
e_B	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0°	7°	15°	0°	7°	15°

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACEx®
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
EcoSPARK®
EfficentMax™
EZSWITCH™ *
EZ™
F®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
MotionMax™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
PDP SPM™
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
Saving our world, 1mW at a time™
SmartMax™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS™
SyncFET™
SYSTEM GENERAL®
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
µSerDes™
µ SerDes
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™

* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I34